Claim 20, line 3, after "port" insert --select--.

Claim 24, line 1, change "3" to --23--.

Claim 24, line 14, before "state" insert --second--.

Please rewrite claims 1, 11, 19, 21, 25, 30, and 33 in amended form as follows:

1. (Twice Amended) A bus system, comprising:

(a) a plurality of bus elements, with each of the plurality of bus elements being capable of making a request for access to at least one other bus element;

(b) a central unit having a plurality of bus inputs and an output, with the central unit being capable of coupling at least one of the inputs to the output, the central unit adapted to provide for an arbitrated, point-to-point coupling of a particular one of the plurality of bus elements with the at least one other bus element;

(c) a first plurality of uni-directional point-to-point buses for coupling in a first predetermined direction the bus elements to the central unit bus inputs;

(d) a second plurality of uni-directional point-to-point buses for coupling in a second predetermined direction the output of the central unit to each of the bus elements; and

(e) arbitration logic connected to the plurality of bus inputs of the central unit to which the first plurality of uni-directional point-to-point buses connect, the arbitration logic being capable of [for] granting each of the bus elements access to the at least one other bus element through the central unit one at a time based upon the requests from the bus elements.

11. (Amended) A system as recited in claim 10, wherein the OR logic comprises:

a first OR gate which has as inputs the first buses from the plurality of central processing units, with the output of the first OR gate being coupled to the second bus for the shared memory; and

a second OR gate which has as a first input the output of the first OR gate and as a second input the first bus from the shared memory, with the output of the second OR gate being coupled to the second buses for [to] the plurality of central processing units.

19. (Amended) The system as recited in claim 18, wherein the system further includes port logic that connects each of the first buses from the plurality of central processing units to the first multiplexer.

21. (Amended) The system as recited in claim 20, wherein the arbitration logic includes an arbitrator coupled to the validity logic, and scheduling logic coupled to the port multiplexer and the arbitrator.

25. (Amended) The system as recited in claim 24, wherein each of the first buses includes at least one function code (FC) line indicative of the beginning and end of a transmission on the bus and wherein the port select logic is responsive to the [control] at least one function code (FC) line to switch the schedule port ID multiplexer to the next port.

30. (Twice Amended) A system comprising:

a plurality of central processing units;

a shared memory;

a central unit including:

combining logic for accepting a plurality of parallel inputs, the plurality of parallel inputs at least equal to the number of the central processing units plus memory and coupling at least one of inputs to its output;

arbitration logic coupled to the combining logic for controlling which of the inputs is provided at the output;

a memory controller providing a memory input to the combining logic and receiving a memory output from the combining logic;

a plurality of first uni-directional point-to-point buses, with one bus coupling each of the central processing units to an input of the combining logic, and with each of the first uni-directional point-to-point buses for coupling in a first predetermined direction a central processing unit to an input of the combining logic;

a first uni-directional memory bus for coupling in a second predetermined direction the memory to the memory controller;

a plurality of second uni-directional point-to-point buses for coupling in a third predetermined direction the output of the combining logic to the central processing units; and

a second uni-directional memory bus for coupling in a fourth predetermined direction the output of the memory to the memory control logic.

33. (Twice Amended) A method of implementing a high speed bus to which a plurality of bus elements are coupled comprising the steps of: